Refine Search

Search Results -

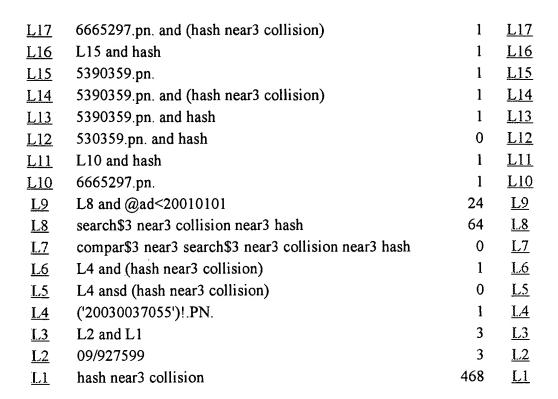
Term	Documents
(27 AND 29).PGPB,USPT.	0
(L29 AND L27).PGPB,USPT.	0

Database:	US Pre-Grant Publication Full-Text Database US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins	
Search:	L30	Refine Search
	Recall Text Clear	Interrupt

Search History

DATE: Monday, June 07, 2004 Printable Copy Create Case

Set Nameside by side		Hit Count Set Name result set	
DB=P	GPB,USPT; PLUR=YES; OP=ADJ		
<u>L30</u>	L29 and L27	0	<u>L30</u>
L29	comparing near3 search value	33	L29
<u>L28</u>	L27 and (comparing near6 (hash near3 collisions))	0	<u>L28</u>
L27	('6735670' '6473846' '6226710')!.PN.	3	<u>L27</u>
L26	L24 and @ad<20010101	19	<u>L26</u>
L25	L24 and ad<20010101	35	L25
L24	L23 and (hash near3 collision)	35	L24
L23	CAM near2 memory	2931	<u>L23</u>
L22	CAM near3 memory	3295	<u>L22</u>
<u>L21</u>	L20 and @ad<20010101	76	<u>L21</u>
<u>L20</u>	L19 near3 L18	113	<u>L20</u>
<u>L19</u>	collision	70848	<u>L19</u>
<u>L18</u>	CAM	215243	<u>L18</u>



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CSTIGO	1 Study of an efficient simulation method Chang, YR.; Computers and Digital Techniques, IEE Proceedings-, Volume: 146, Issue: 5, Sept. 1999 Pages:253 - 258 [Abstract] [PDF Full-Text (428 KB)] IEE JNL
Web Account O- Access the IEEE Member Digital Library	2 GaAs VLSI implementation of a 2.5 Gb/s ATM label translator Moussa, I.; Lassen, P.S.; Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1996. Technical D 1996., 18th Annual, 3-6 Nov. 1996 Pages:69 - 72 [Abstract] [PDF Full-Text (520 KB)] IEEE CNF
	3 Looking for analogues in structural safety management through connectionist associative memories Lazzari, M.; Salvaneschi, P.; Brembilla, L.; Neural Networks for Identification, Control, Robotics, and Signal/Image Proce 1996. Proceedings., International Workshop on , 21-23 Aug. 1996 Pages:392 - 400 [Abstract] [PDF Full-Text (476 KB)] IEEE CNF

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1 An associative file store using fragments for run-time indexing and compression R. M. Lea, E. J. Schuegraf



June 1980 Proceedings of the 3rd annual ACM conference on Research and development in information retrieval

Full text available: 📆 odi(690.98 K8) — Additional Information: full odation, references

2 A high performance transparent bridge Martina Zitterbart, Ahmed N. Tantawy, Dimitrios N. Serpanos August 1994 IEEE/ACM Transactions on Networking (TON), Volume 2 Issue 4

Additional Information: full citation, references, index terms Full text available: Sdf(1.41 MB)

3 A microprogrammed keyword transformation unit for a database computer Krishnamurthi Kannan, David K. Hsiao, Douglas S. Kerr October 1977 Proceedings of the 10th annual workshop on Microprogramming

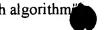
Full text available: pdf(705.09 K8) Additional Information: full citation, abstract, references, citings, index terms

The design of a microprogrammable microprocessor-based keyword transformation unit for a database computer(DBC) is described. The DBC, a specialized back-end computer capable of managing 109 - 1010 bytes of data, consists of two loops of memories and processors, the structure loop and the data loop, connected through a database command and control processor (DBCCP). The structure loop is used to retrieve and update the large amount (10

4 LH*—a scalable, distributed data structure Witold Litwin, Marie-Anna Neimat, Donovan A. Schneider December 1996 ACM Transactions on Database Systems (TODS), Volume 21 Issue 4

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(780.53 KB) terms, review

We present a scalable distributed data structure called LH*. LH* generalizes Linear Hashing (LH) to distributed RAM and disk files. An LH* file can be created from records with primary keys, or objects with OIDs, provided by any number of distributed and autonomous clients. It does not require a central directory, and grows gracefully, through splits of one bucket at a time, to virtually any number of servers. The number of messages per random insertion is one in general, and three in the w ...



Keywords: algorithms, data structures, distributed access methods, extensible hashing, linear hashing

	FLATS, a machine for numerical, symbolic and associative computing Eiichi Goto, Tetsuo Ida, Kei Hiraki, Masayuki Suzuki, Nobuyuki Inada April 1979 Proceedings of the 6th annual symposium on Computer architecture	
	Full text available: pdf(515,62 KB) Additional Information: full cliation, abstract, references, index terms	
	Functional aspects of a machine called FLATS are described. FLATS aims to efficiently run both numerical and algebraic programs. Overflow free and variable precision arithmetic, table look-up computation, and associative computation based on single-hit content addressed tables are introduced for advanced numerical, algebraic and symbolic computing. Hashing hardware, tag mechanism and hardware list processing are used to realize these features.	
	An associative/parallel processor for partial match retrieval using superimposed codes Sudhir R. Ahuja, Charles S. Roberts May 1980 Proceedings of the 7th annual symposium on Computer Architecture	******
	Full text available: pdf(853.16 KB) Additional Information: full citation, abstract, references, citings, index terms	
	This paper presents the design and implementation of special hardware for effective use of the method of superimposed codes. It is shown that the method of superimposed codes is particularly well suited to easy design and implementation of fast and modular hardware. The implementation has shown that a performance gain of two orders of magnitude over conventional software implementations is obtained by using the special hardware. This makes the method of superimposed codes extremely attracti	
7	A multi-user data flow architecture F. J. Burkowski	*****
	May 1981 Proceedings of the 8th annual symposium on Computer Architecture Full text available: ndf(606.85 KB) Additional Information: full cliation, abstract, references, citings, index terms	
	This paper discusses the design of a prototype data flow machine that has memory management hardware in each memory block. This facility allows loading and deleting code that is produced by independent compilations. The first sections of the paper deal with the general architecture of the machine and the format specifications for the instruction cells, logical addresses, and switch packets. The paper concludes with a discussion of the mapping hardware used in the memory blocks. The results	
8	Design of a high-performance ATM firewall Jun Xu, Mukesh Singhal November 1998 Proceedings of the 5th ACM conference on Computer and	*****
	communications security	
	communications security Full text available: df(1.27 MB) Additional Information: full citation, references, index terms Trading packet headers for packet processing Girish P. Chandranmenon, George Varghese	
	communications security Full text available: def(1.27 MB) Additional Information: full citation, references, index terms Trading packet headers for packet processing	